

1/2

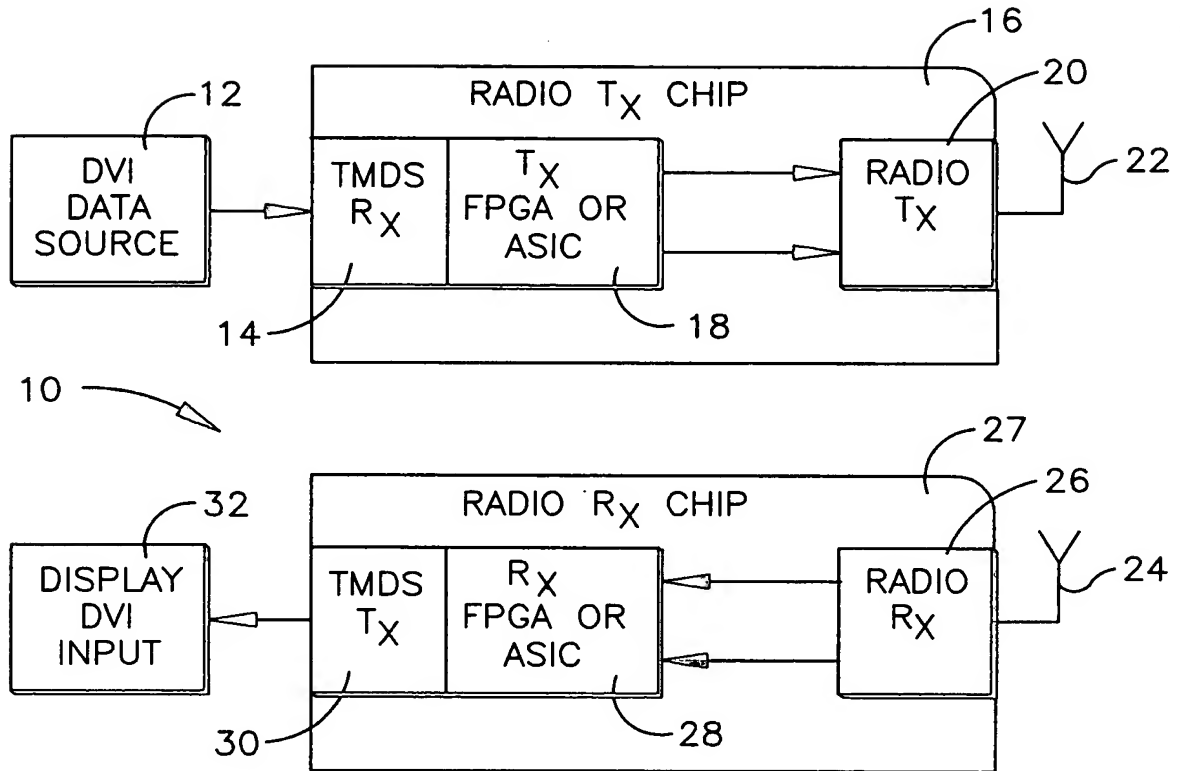


Fig. 1

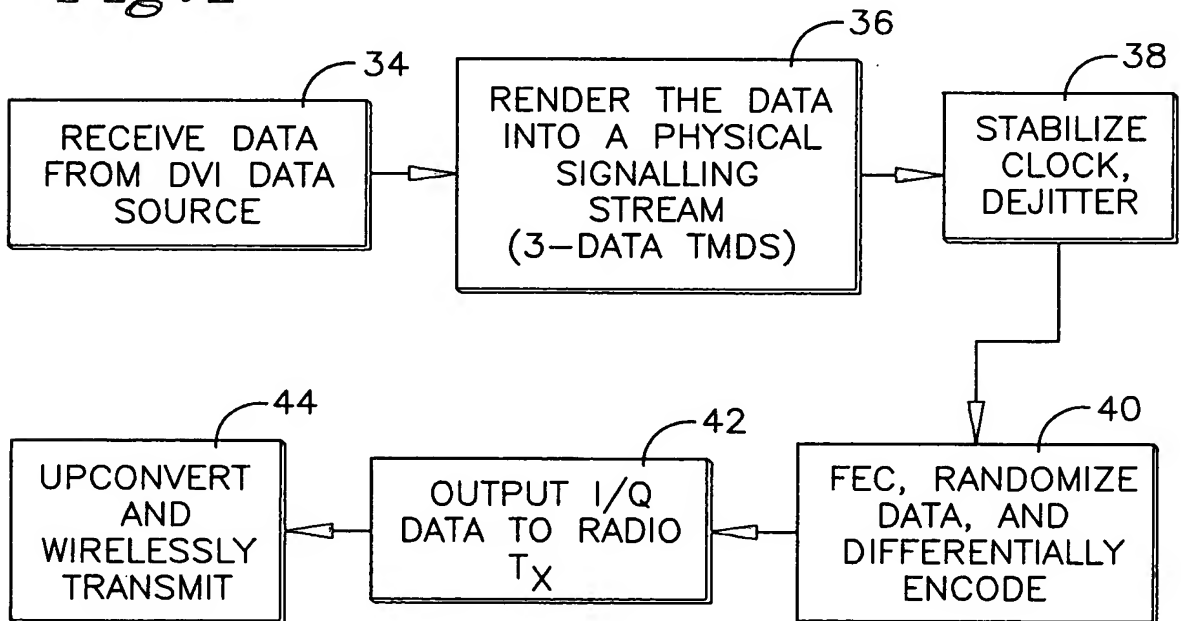


Fig. 2

TRANSMITTER LOGIC

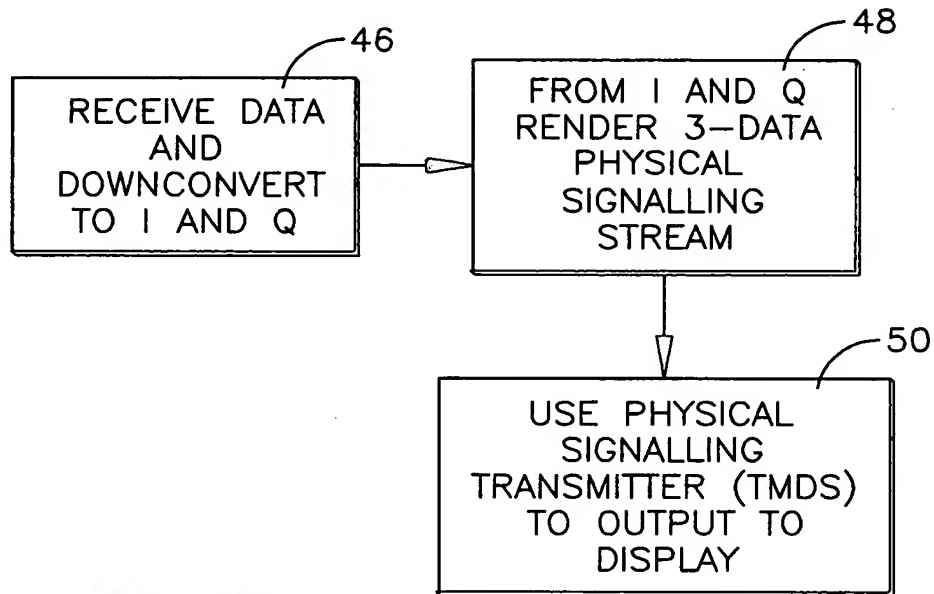


Fig. 3
RECEIVER LOGIC